**Digital Logic Design – Multiplexer Practice Problems**

**Question 1:** Design a 16X1 MUX using decoder and basic gate(s).

**Question 2:** Implement a ***17 to 1*** MUX using only 4 to 1 MUX(s) and 2x1 MUX(s).

**Question 3:** Design a quad 4x1 MUX using four 4x1 MUX(s).

**Question 4:** Design ***Quad 4-to-1*** MUX using 2-to-1 MUX(s).

**Question 5:** Design Dual 3x1 MUX using two 2x1 MUX and one dual 2x1 MUX.

**Question 6:** Design a Dual 16x1 MUX using

1. Four Dual 4x1 MUX(s) and three Dual 2x1 MUX(s) only
2. Five Dual 4x1 MUX(s) only

**Question 7:** (a) Implement the following function with MUX, and other necessary logic gates

F(A,B,C,D) = ∑ m (0,1,3,4,8,9,15)

(b) Now, implement the above function using A as data input and B, C, D as selectors.

(c) Realize the above function using 4x1 MUX and external gating.

**Question 8:** A combinational circuit is defined by the following functions:

F1= x'.y' + x.y.z'

F2= x' +y

F3= x.y + x'.y'

Implement above functionality using MUX(s) and external gates.

**Question [9-13]:** Text Book exercises 3-39, 3-40 (12x3 AND-OR means 12 AND gates each taking 3 inputs), 3-41, 3-42, 3-46

**Question 14: Short Questions**

1. What will be the output of multiplexer for the information given below:

|  |  |  |  |
| --- | --- | --- | --- |
| **MUX Size** | **Information Input (I)** | **Selection Input (S)** | **Output (Y)** |
| 16-to-1 | 1101010111000110 | 0110 |  |
| 16-to-1 | 1101010111000110 | 1001 |  |
| 8-to-1 | 11010101 | 101 |  |
| Quad 2-to-1 | 1011  1001 | 0 |  |
| Dual 4-to-1 | 10  11  01  00 | 11 |  |
| Quad 8-to-1 | 1001  0111  1010  0001  1111  1000  0101  0110 | 110 |  |

1. Write equation (in any form) of Function given below without using truth table.

|  |  |
| --- | --- |
| For the given MUX,  S (X,Y,Z) = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  C (X,Y,Z) = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  (Write equation in any form) |  |